

## CLAIMS

1           1.     A method for processing a microelectronic substrate, comprising:  
2                 providing a microelectronic substrate having a first surface and a second  
3 surface facing a direction opposite from the first surface;  
4                 forming a plurality of voids in the microelectronic substrate, each void  
5 having an open end at the first surface and extending from the first surface to a separation  
6 region between the first and second surfaces;  
7                 forming at least one operable microelectronic device at and/or proximate to  
8 the first surface of the microelectronic substrate; and  
9                 separating a first stratum of the microelectronic substrate above the  
10 separation region from a second stratum of the microelectronic substrate below the  
11 separation region.

1           2.     The method of claim 1, further comprising:  
2                 at least partially filling the voids with a filler material to close the open end  
3 of the voids;  
4                 constructing a film on the first surface of the first substrate; and  
5                 forming at least one operable microelectronic device in the film.

1           3.     The method of claim 1 wherein forming the voids includes forming  
2 tapered voids having a first void area transverse to the first surface of the substrate at the  
3 first surface and a second void area transverse to the first surface of the substrate below  
4 the first surface, the second void area being larger than the first void area.

1           4.     The method of claim 3 wherein forming the tapered voids includes  
2 disposing an etchant on the first surface of the substrate and tilting the substrate.

1                   5.     The method of claim 3 wherein forming the tapered voids includes  
2 directing an energy beam toward the first surface of the substrate and tilting the substrate  
3 as the energy beam impinges on the first surface.

1                   6.     The method of claim 1, further comprising forming each of the voids  
2 to have approximately the same depth beneath the first surface so that the separation  
3 region is generally flat.

1                   7.     The method of claim 1, further comprising closing entrance openings  
2 of the voids at the first surface of the substrate by at least partially filling the voids.

1                   8.     The method of claim 1 wherein the substrate includes a die having a  
2 transverse dimension at the first surface, further comprising spacing adjacent voids by a  
3 distance less than the transverse dimension.

1                   9.     The method of claim 1 wherein separating the first stratum of the  
2 microelectronic substrate from the second stratum includes applying a force to the first  
3 stratum in a selected direction to break connecting portions of the microelectronic  
4 substrate coupling the first and second strata of the microelectronic substrate between the  
5 voids.

1                   10.    The method of claim 9, further comprising varying a magnitude of  
2 the force while engaging the first stratum of the microelectronic substrate.

1                   11.    The method of claim 9 wherein the separation region defines a plane  
2 and applying a force includes applying a force in a direction parallel to the plane.

1                   12.    The method of claim 9 wherein the separation region defines a plane  
2 and applying a force includes applying a force in a direction transverse to the plane.

1                    13.    The method of claim 9, further comprising releasably engaging the  
2 first surface of the microelectronic substrate by applying a suction force to the first  
3 surface.

1                    14.    The method of claim 1 wherein forming at least one microelectronic  
2 device includes forming first microelectronic devices defining a first microelectronic die  
3 and forming second microelectronic devices defining a second microelectronic die.

1                    15.    The method of claim 1, further comprising selecting the substrate to  
2 include silicon.

1                    16.    The method of claim 1, further comprising selecting the substrate to  
2 include a wafer.

1                    17.    The method of claim 16, further comprising selecting the wafer to  
2 have a diameter of from about eight inches to about twelve inches.

1                    18.    The method of claim 1, further comprising venting gases through the  
2 voids.

1                    19.    The method of claim 1, further comprising aligning the voids along a  
2 line separating adjacent dies.

1                    20.    The method of claim 1, further comprising merging at least a portion  
2 of one void with a portion of an adjacent void.

1                    21.    The method of claim 1, further comprising at least partially  
2 separating a first die of the substrate from an adjacent second die of the substrate by  
3 aligning the voids between the dies.

1                   22. A method for forming a plurality of microelectronic dies,  
2 comprising:  
3                   providing a substrate having a first surface and a second surface facing a  
4 direction opposite the first surface;  
5                   perforating the substrate at a separation region by forming a plurality of  
6 voids in the first substrate, the voids having an open end at the first surface with a first  
7 transverse dimension and a closed end at the separation region between the first and  
8 second surfaces, the closed end having a second transverse dimension greater than the  
9 first transverse dimension;  
10                  constructing a film on the first surface of the substrate;  
11                  forming a plurality of microelectronic devices in and/or on the film to  
12 define first and second microelectronic dies;  
13                  separating the first die from the second die by cutting through the film in a  
14 direction transverse to a plane of the separation region; and  
15                  separating the first and second dies from the substrate along the separation  
16 region.

1                   23. The method of claim 22 wherein the substrate includes a first lattice  
2 structure and the film includes a second lattice structure, further comprising aligning the  
3 second lattice structure with the first lattice structure.

1                   24. The method of claim 22, further comprising selecting the film to  
2 have a chemical composition the same as a chemical composition of the substrate.

1                   25. The method of claim 22 wherein separating the first die from the  
2 second die includes disposing a blade between the first and second dies.

1                   26. The method of claim 22 wherein the first die separates from the  
2 second die before the first and second dies separate from the substrate.

1                   27.    The method of claim 22, further comprising closing the open ends of  
2   the voids at the first surface of the substrate by at least partially filling the voids before  
3   disposing the film on the substrate.

1                   28.    The method of claim 22 wherein separating the first die from the  
2   second die includes merging voids positioned between the first and second dies.

1                   29.    The method of claim 22 wherein separating the first and second dies  
2   from the substrate includes applying a suction cup to the first die, at least partially  
3   evacuating the suction cup, and applying a force to the first die in a selected direction to  
4   break connecting portions of the substrate coupling the die to the substrate between the  
5   voids.

1                   30.    The method of claim 29, further comprising varying a magnitude of  
2   the force while engaging the first die.

1                   31.    The method of claim 29 wherein applying a force includes applying  
2   a force transverse to a plane of the separation region.

1                   32.    The method of claim 22, further comprising spacing the voids apart  
2   by a distance less than a transverse dimension of the first die.

1                   33.    A microelectronic die, comprising:  
2                   a substrate having a first external surface, a second external surface facing a  
3   direction opposite from the first external surface, and a thickness between the first and  
4   second external surfaces of less than about 150 microns; and  
5                   at least one operable microelectronic device at least proximate to one of the  
6   external surfaces.

1           34.    The microelectronic die of claim 33 wherein the second external  
2 surface includes a plurality of blind voids extending from the second surface toward the  
3 first surface, the voids having an open end at the second surface and a closed end  
4 between the second and first surfaces.

1           35.    The microelectronic die of claim 34 wherein the voids are etched  
2 voids.

1           36.    A microelectronic die, comprising:  
2                a substrate having a first external surface, a second external surface facing a  
3 direction opposite from the first external surface, and a plurality of voids extending from  
4 the second external surface toward the first external surface; and  
5                a plurality of operable microelectronic devices proximate to the first  
6 surface.

1           37.    The microelectronic die of claim 36, wherein the first external  
2 surface is separated from the second external surface by about 150 microns or less.

1           38.    The microelectronic die of claim 36 wherein the voids are tapered  
2 and are larger toward the second external surface of the substrate than toward the first  
3 external surface.

1           39.    The microelectronic die of claim 36 wherein the voids are etched  
2 voids.

1           40.    The microelectronic die of claim 36 wherein the voids are regularly  
2 spaced apart from each other.

1           41.    The microelectronic die of claim 39 wherein the voids are randomly  
2 spaced apart from each other.

1                   42.    A microelectronic substrate for forming one or more microelectronic  
2 dies, the substrate comprising:

3                   a substrate body having a first surface and a second surface facing a  
4 direction opposite the first surface; and

5                   a plurality of sidewalls in the substrate body, each sidewall defining a void  
6 within the substrate body, each void having a first end at the first surface of the substrate  
7 body and a second end at a separation region between the first and second surfaces of the  
8 substrate body.

1                   43.    The substrate of claim 42, further comprising at least one operable  
2 microelectronic device at and/or proximate to the first surface of the substrate body.

1                   44.    The substrate of claim 42 wherein each void is a blind void with the  
2 second end being a closed end, further wherein the first end of each void is filled with a  
3 filler material.

1                   45.    The substrate of claim 42 wherein the substrate body includes  
2 silicon.

1                   46.    The substrate of claim 42 wherein the substrate body includes a  
2 wafer having a diameter of from about eight inches to about twelve inches.

1                   47.    The substrate of claim 42, further comprising a film layer disposed  
2 on the first surface of the substrate body.

1                   48.    The substrate of claim 47 wherein the film has an external surface  
2 facing an opposite direction from the second surface of the substrate body, further  
3 wherein a distance between the external surface and the separation region is less than  
4 about 150 microns.

1           49.    The substrate of claim 42 wherein the voids are tapered with the first  
2   end of each void smaller than the second end of each void.

1           50.    The substrate of claim 42 wherein the voids include first and second  
2   voids extending to approximately the same depth beneath the first surface, further  
3   wherein the separation region defines a generally flat plane.

1           51.    The substrate of claim 42, further comprising:  
2           a first operable microelectronic device in a first die portion at and/or  
3   proximate to the first surface of the substrate body; and  
4           a second operable microelectronic device in a second die portion at and/or  
5   proximate to the first surface of the substrate body, the second die portion being  
6   separable from the first die portion.

1           52.    A microelectronic substrate, formed by the process comprising:  
2           providing a substrate having a first surface and a second surface facing a  
3   direction opposite from the first surface;  
4           forming a plurality of voids in the substrate, each void extending from the  
5   first surface to a separation region between the first and second surfaces;  
6           forming at least one operable microelectronic device at and/or proximate to  
7   the first surface of the substrate; and  
8           separating a first stratum of the microelectronic substrate above the  
9   separation region from a second stratum of the microelectronic substrate below the  
10   separation region.

1           53.    The substrate of claim 52 wherein forming the first stratum includes  
2   forming the first stratum to have a thickness of less than about 150 microns measured  
3   from the first surface to the separation region.

1           54.    The substrate of claim 52, further comprising:



2                   at least partially filling the voids with a filler material to close an open end  
3 of the voids at the first surface of the substrate;  
4                   disposing a film on the first surface of the substrate; and  
5                   forming the microelectronic device in the film.

1                   55. The substrate of claim 52 wherein forming the voids includes  
2 forming tapered voids having a first void area transverse to the first surface of the  
3 substrate at the first surface and a second void area transverse to the first surface of the  
4 substrate below the first surface, the second void area being larger than the first void area.

1                   56. The substrate of claim 52, further comprising forming the voids to  
2 have approximately the same depth beneath the first surface so that the separation region  
3 is generally flat.

1                   57. The substrate of claim 52, further comprising closing entrance  
2 openings of the voids at the first surface of the substrate by at least partially filling the  
3 voids.

1                   58. The substrate of claim 52 wherein forming the voids includes  
2 forming tapered voids by disposing an etchant on the first surface of the substrate and  
3 tilting the substrate.

1                   59. The substrate of claim 52 wherein forming the voids includes  
2 forming tapered voids by directing an energy beam toward the first surface of the  
3 substrate and tilting the substrate as the energy beam impinges on the first surface.

1                   60. The substrate of claim 52, further comprising spacing adjacent voids  
2 by a distance less than a transverse dimension of a die formed from the substrate.

1                   61. The substrate of claim 52 wherein separating the first stratum of the  
2 microelectronic substrate from the second stratum includes applying a force in a selected

3 direction to the first stratum to break connecting portions of the microelectronic substrate  
4 coupling the first and second strata of the microelectronic substrate between the voids.

1 62. The substrate of claim 61, further comprising varying a magnitude of  
2 the force while engaging the first stratum of the microelectronic substrate.

1 63. The substrate of claim 61 wherein applying a force includes applying  
2 a force in a direction parallel to a plane of the separation region.

1 64. The substrate of claim 61 wherein applying a force includes applying  
2 a force transverse to a plane of the separation region.

1 65. The substrate of claim 61, further comprising releasably engaging  
2 the first surface of the substrate by applying a suction force to the first surface.

1 66. The substrate of claim 52 wherein forming at least one  
2 microelectronic device includes forming first microelectronic devices defining a first  
3 microelectronic die and forming second microelectronic devices defining a second  
4 microelectronic die.

1 67. The device of claim 52, further comprising selecting the substrate to  
2 include a silicon wafer.

1 68. The device of claim 67, further comprising selecting the wafer to  
2 have a diameter of from about eight inches to about twelve inches.